REMARKS

Claims 1-25 are pending in this application, of which claim 6 has been amended. Claims 1-5, 8, 10 and 17-25 are withdrawn from consideration. No new claims have been added.

Claims 6, 9 and 14-15 stand rejected under 35 U.S.C. § 103(a) as unpatentable over U.S. Patent Publication 2005/0045947 to Chen et al. (hereafter "**Chen et al.**").

Applicants respectfully traverse this rejection.

Chen et al. discloses a field effect transistor (FET), integrated circuit (IC) chip including the FETs and a method of forming the FETs. The devices have a thin channel, e.g., an ultra-thin (smaller than or equal to 10 nanometers (10 nm) silicon on insulator (SOI) layer. Source/drain regions are located in recesses at either end of the thin channel and are substantially thicker (e.g., 30 nm) than the thin channel. Source/drain extensions and corresponding source/drain regions are self aligned to the FET gate and thin channel.

In claim 6 of the present invention, a laminated region of a sacrificial layer and a semiconductor layer formed on the sacrificial layer is formed, and the sacrificial layer is removed through the opening to form a cavity below the semiconductor layer.

On the other hand, in **Chen et al.**, a thin insulator layer 148 is formed between an ultra-thin channel layer 150 and a sacrificial layer 146. The thin insulator layer 148 separates the ultra-thin channel layer 150 from the sacrificial layer 146 (see paragraph [0028] of **Chen et al.**). However, the thin insulator layer 148 does not play a role as a sacrificial layer, but the thin insulator layer 148 remains on the whole or part of the bottom surface of a semiconductor layer

in order to form a channel 172 and recessed source/drain and extension areas 180.

In claim 6, as amended, it is not necessary that (whole or part of) any layer remains on the bottom surface of a semiconductor layer when a cavity is formed. Further, **Chen et al.** does not disclose or suggest removing the whole of the sacrificial layer formed below the semiconductor layer and forming a cavity below the semiconductor layer as shown in claim 6, as amended.

Thus, the 35 U.S.C. § 103(a) rejection should be withdrawn.

Claim 16 stands rejected under 35 U.S.C. § 103(a) as unpatentable over **Chen et al.** in view of U.S. Patent 6,881,635 to Chidambarrao et al. (hereafter "**Chidambarrao et al.**").

Applicants respectfully traverse this rejection.

Chidambarrao et al. discloses a planar NFET on a strained silicon layer supported by a SiGe layer which achieves reduced external resistance by removing SiGe material outside the transistor body and below the strained silicon layer and replacing the removed material with epitaxial silicon, thereby providing lower resistance for the transistor electrodes and permitting better control over Arsenic diffusion.

Chidambarrao et al., like **Chen et al.** discussed above, fails to teach, mention or suggest the step of removing the whole of the sacrificial layer formed below the semiconductor layer and forming a cavity below the semiconductor layer, as recited in claim 6, as amended, from which claim 16 depends.

Thus, the 35 U.S.C. § 103(a) rejection should be withdrawn.

The Examiner has indicated that claims 7 and 11-13 would be allowable if rewritten in

independent form.

Applicants respectfully defer such action until a FINAL Office Action, if any, is received.

In view of the aforementioned amendments and accompanying remarks, claims 6, 7, 9 and 11-16, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, KRATZ, QUINTOS,
HANSON & BROOKS, LLP

William L. Brooks
Attorney for Applicant
Reg. No. 34,129

WLB/ak
Atty. Docket No. **040126**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

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